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Strength and fracture analysis of silicon-based components for embedding

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Abstract

Single-crystalline silicon chips are widely employed in printed circuit boards (PCBs) as embedded components. Their design often requires one side patterned with metal contacts, whereas the opposite one is constituted by pure silicon. These components must possess a minimum strength to withstand the loads occurring during both production and operation of the board. In this work, the strength and fracture behaviour of miniaturised Si chips (dimensions: 2 mm × 2 mm × 0.125 mm) has been assessed under biaxial loading on both the pure silicon side and the metal-patterned side by means of a miniaturised ball-on-three-balls (B3B) fixture. Experimental results showed significant difference in the characteristic fracture load between the silicon-side ($P_0 = 21.2$ N, Weibull modulus $m \approx 2.6$) and the metal-patterned side ($P_0 = 8.6$ N, $m \approx 12.3$). Fracture mechanics and fractographic analyses, together with FE simulations of the loading process, helped clarifying the effect of the metal contacts on the overall fracture behaviour of the Si-chips.

Keywords: B. Failure analysis; C. Fracture; C. Strength; E. Functional applications; Printed circuit boards

1. Introduction

Innovation and improved added value in advanced printed circuits board (PCB) technology are mainly driven by miniaturisation, better performance, and reduction in cost.[1,2] The development of the embedding concept, in contrast to the common surface-mount technology (SMT) circuits, is a direct consequence of these aspects. In SMT both passive and active components of electric circuits are assembled and soldered onto the surface of the PCB, whereas embedded discrete components are directly included within the board. Some of the advantages in using the embedding concept are the reduction in surface area by moving functional components from the surface into the inner layers, which results in more circuits per fabrication panel. In addition, the necessary length of interconnections is reduced, thus higher speeds and lower electrical signal noise can be achieved.[1] This process requires tailoring of the PCB layer architecture, positioning of the embedding components and subsequent thermal pressing of the package. In this regard, high mechanical reliability of components is generally required for the embedding process. The embedded devices (*e.g.* ceramic capacitors or silicon chips) are very brittle and the force required to fracture them can be of the order of few Newtons. In addition, placing the components inside the PCB introduces new sources of residual stress and increases the complexity of the stress field during fabrication (*i.e.* thermo-mechanical pressing) of the PCB. During the embedding process, for instance, temperatures may reach 200–250 °C and the applied pressures can be as high as 30 MPa (mean set up in the pressing die). In this regard, the lateral flow of the polymeric material during pressing and the thermal expansion coefficient mismatch during cooling produces residual stresses to a level that cracking and/or delamination might be induced in the components. In addition, the non-symmetrical structure of components and their location (either near the top or at the bottom of the package) yield a complex stress distribution within and around the component during thermal pressing and subsequent cooling down to room temperature. Furthermore, thermo-mechanical stresses may occur during operation of the board. Hence, the functionality of the entire package also relies on the mechanical strength of the individual components.

Semiconductor silicon chips are among the most commonly employed embedded components. Their design often requires

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one side patterned with metal contacts, whereas the opposite one is constituted by pure silicon. Thus, embedding can be performed either with the metal-patterned side upwards or downwards, with respect to the upper surface of the board. Due to the aforementioned thermo-mechanical loads during the embedding process, the plate- or disk-like geometry of the embedded component can lead to the bending of the component itself during packaging. Since the mechanical properties of each surface might differ due to different finishing and architectural features,[3] different levels of mechanical reliability of the board may be attained depending on whether the pure silicon side or the metal-patterned side is exposed to tensile stresses. The functionality of the board relies significantly on the survival of the embedded components, and thus the evaluation of mechanical properties is of primary importance in order to estimate the performance limits of the entire package.

Mechanical testing is generally carried out with biaxial fixtures, and the brittle nature of many components (*e.g.* silicon) employed for embedding makes the use of Weibull statistics necessary for strength determination.[4,5] Common methods described in the literature for the mechanical testing of plate-shaped specimens are modifications of the ring-on-ring (ROR) flexure concept.[3,6] However, it has been shown that during these tests small geometric inaccuracies can lead to an undefined load transfer from the rings to the specimen and thus cause large uncertainties in the determined strength.[7,8] This is specially enhanced when testing small specimens. In this regard, such uncertainties can be minimised when a different loading configuration, the ball-on-three-balls (B3B) test, is used.[9–11] Despite the small effective volume tested with this method, localised strength measurements (*i.e.* near metal contacts, vias, etc.) can be performed even in miniaturised (*e.g.* less than 0.5 mm^3) components[12]. Thus, the influence of micro-sized surface features on strength can be assessed to determine the reliability of the embedded component.

The purpose of the present investigation is to determine the strength and fracture characteristics of silicon components to be embedded into PCBs. Strength measurements are performed using a miniaturised B3B testing jig on very thin 2 mm × 2 mm plate-like single-crystalline silicon specimens. The experimental results are interpreted using Weibull statistics, fracture mechanics concepts supported by chemical and fractographic analyses, and FE simulations of the stress distribution during loading. The influence of the nature of the metal–silicon interface, the defect population and the presence of interface-driven stress concentrations on the strength of the components is discussed.

2. Materials and methods

2.1. Single crystalline silicon chips

Silicon chips derived from single crystalline wafers were supplied by AT&S (Leoben, Austria) in the form of 2 mm × 2 mm platelets. The chips presented two different sides: one constituted by mirror-polished pure silicon and the other side with deposited metal contacts and interconnects, as shown in Fig. 1a and b. The two surfaces will henceforth be referred to as "Si-side" and "metal-side", respectively. The thickness of the chips was measured with a digital test gauge (DIGIMET, Helios-Preissler, Gammertingen, Germany), resulting in 0.125 ± 0.010 mm. The uncertainty on the thickness measurement was due to the presence of the metal contacts on the metal-side.

The crystallographic directions of the Si chips, as indicated in Fig. 1a and b, were identified with the aid of electron back-scattered diffraction (EBSD). The EBSD system used was an EDAX equipped with OIM software (EDAX, Mahwah, NJ, USA), installed on a Field Emission Gun Scanning Electron Microscope (FEG-SEM: LEO Gemini 1525, Carl Zeiss, Oberkochen, Germany). Electron Probe Micro-Analyses (EPMA) were performed with a JEOL JXA-8530F Field Emission EPMA (JEOL, Tokyo, Japan) used only in the energy dispersive mode.

2.2. The ball-on-three-balls (B3B) method

The strength of the Si-chips was determined using a miniaturised B3B fixture especially built in-house to match the dimensions of the supplied components (*cf.* Fig. 1c). In the B3B method, a rectangular plate (or a disc) is symmetrically supported by three balls on one side and loaded by a fourth ball in the centre of the opposite side, which produces a very well defined biaxial stress field.[9–11] The load is increased until fracture occurs, and the fracture load can be used to calculate the maximum tensile biaxial stress in the specimen at the moment of fracture. For a bulk plate of an elastically isotropic material the equivalent maximum stress σ_{max} corresponding to the fracture load P can be calculated as follows:

$$\sigma_{max} = f\frac{P}{t^2}, \quad (1)$$

where t is the specimen thickness, and f is a dimensionless factor which depends on the geometry of the specimen, on the Poisson's ratio of the tested material, and on the details of the load transfer from the jig into the specimen.

All B3B tests were carried out in a universal testing machine (Zwick Z010, Zwick/Roell, Ulm, Germany). In order to reproduce the possible stress states occurring during the embedding process, two testing configurations were adopted: (i) pure silicon surface under tension (Si-side) and (ii) surface with metal contacts and interconnects under tension (metal-side). Optical examination of fracture surfaces was carried out with an Olympus BX50 light microscope, an Olympus SZH10 stereo microscope (Olympus, Tokyo, Japan), and with a Quanta 200 Mk2 FEG-SEM (FEI, Hillsboro, OR, USA) scanning electron microscope.

2.3. Set-up of FE modelling

A numerical analysis of the system based on a three-dimensional (3D) FE simulation with solid elements (ANSYS rel. 11, ANSYS, Canonsburg, PA, USA) was developed in order to simulate the stress distribution in the entire specimen during biaxial B3B testing. This model has been used to calibrate the

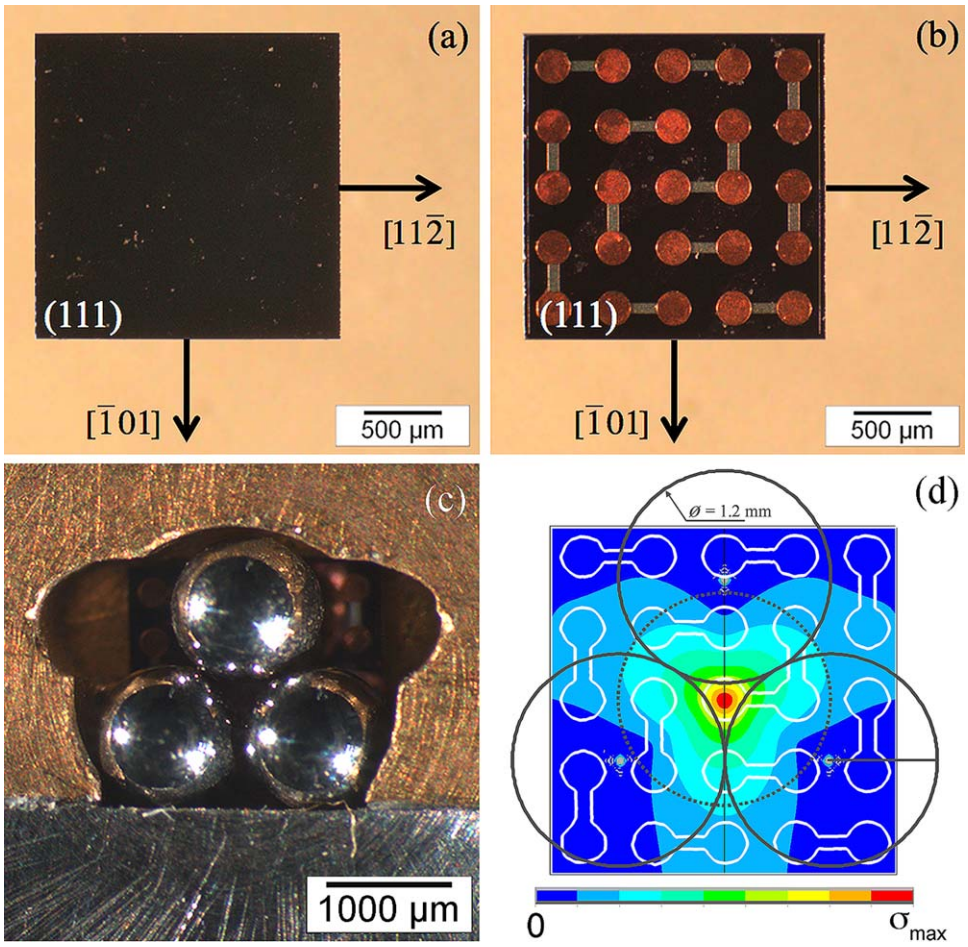

Fig. 1. Micrographs of (a) Si-side and (b) metal-side single crystalline Si-chips for embedding into PCBs. Crystallographic directions are reported as derived from EBSD analysis. (c) Miniaturised B3B fixture used for the biaxial testing of the 2 mm × 2 mm Si-chips. (d) Stress distribution in the Si-chips upon biaxial loading in a B3B fixture (metal-side), as calculated by FE modelling (Eq. (1)). The position of the loading balls is also indicated. The maximum stress is located in correspondence of the central metal contact.

factor f for this configuration, resulting in a value of $f = 2.21$ considering $0.12 < t < 0.13$ (in mm), Poisson's ratio $\nu = 0.3$ and $\text{ø} = 1.2$ mm as diameter of the loading balls. The corresponding stress distribution during loading the Si-chip (on the metal side) in the miniaturised B3B fixture used is represented in Fig. 1d. As can clearly be seen, the maximum stress in the Si-chip is expected within the area covered by the central metal contact.

The use of Eq. (1) to calculate the strength of single-crystalline silicon wafers is indeed a simplified model, which assumes a linear elastic homogeneous material. Nevertheless, FE simulations of the stress distributions for elastically anisotropic silicon plates with various orientations have demonstrated that the error involved using Eq. (1) for silicon single-crystalline plates is always confined within 2% for the maximum stress value. We also caution the reader that the influence of the metal contacts has been neglected for the model, considering the total thickness as the effective thickness (t) for the calculation of the equivalent maximum stresses with Eq. (1).

In addition to the 3D model, a two-dimensional (centrally loaded axisymmetric) sub-model has been developed considering the metal contacts on the top of the specimen and the layers at the interfacial area between metal contacts and silicon. This sub-model aims to determine the influence of metal contacts on the stress distribution around the interfacial area. This 2D choice is justified by the fact that at the centre of the specimen loaded with the B3B fixture a biaxial stress field is produced, and thus a two-dimensional model would allow a simple calculation of stresses in the different layers of the specimen. In this regard, a three-dimensional model would have resulted in much higher calculation times.

The principal geometry of the sub-model is shown in Fig. 2a. The employed dimensions and material parameters are listed in Table 1. Geometrical dimensions and composition of the layers were chosen according to EPMA and SEM analyses of the Si-chip cross-section (Fig. 2b and next section), while the material parameters were taken from the literature.[13,14] Fig. 3a displays the interfacial area. Two different geometries were adopted for modelling; in one case the aluminium buffer layer terminates directly at the passivating oxide layer (Fig. 3b), in the second case the aluminium constitutes an interconnect that stretches along the whole surface (Fig. 3c). Since the main objective of the model is to compare these two configurations, only linear elastic material behaviour was used for the sake of simplicity.

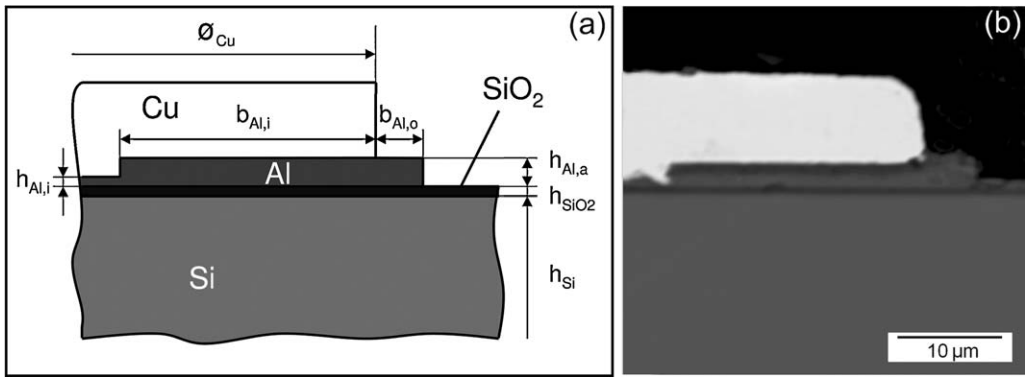

Fig. 2. (a) Description of the geometry adopted for FE sub-modelling of the metal-silicon interface. (b) SEM picture of the edge of the central metal contact on the patterned side of Si-chips.

Based on experimental observations of real geometries, the edge radii of the Cu–Al and Al–SiO_2 (or Al–Al) interfaces (r_{edge}) were chosen as 0.5 μm for all models.

3. Results and discussion

3.1. Biaxial strength results

Fig. 4 shows the results of B3B tests conducted both on the Si-side and the metal-side of single-crystalline Si chips. Data are represented in terms of fracture load (or fracture strength, *cf.* Eq. (1)) vs. the probability of failure. The scale chosen in the graph allows representing Weibull-distributed data as a straight line. Each distribution was collected on a sample of 30 specimens, which ensures statistical significance for the Weibull analysis.[4] Table 2 reports the exact values of the obtained characteristic fracture load P_0 (*i.e.* corresponding to a probability of failure of $F = 63.21\%$) and the corresponding Weibull moduli, m, for both Si-side and metal-side distributions, together with the respective 90% confidence intervals. The equivalent characteristic strength σ_0 and the effective volume for the calculation on the Si-side are also reported in Table 2.

It can be clearly inferred from Fig. 4 that testing Si chips with either the pure silicon or the metal-patterned side under tension produces dramatically different results. In particular, Si-side specimens possess a higher characteristic fracture load than the metal-side ones (*i.e.* 21.2 N vs. 8.6 N). However, the Weibull modulus for the latter is considerably higher (*i.e.* 12.3 vs. 2.6); the specimens break in a very narrow range of stresses (higher mechanical reliability in terms of design). Since the only difference between the two cases was the surface that was subject to biaxial tensile stress, it is clear that there is a strong effect of the deposited metal contacts on the overall strength behaviour of the material.

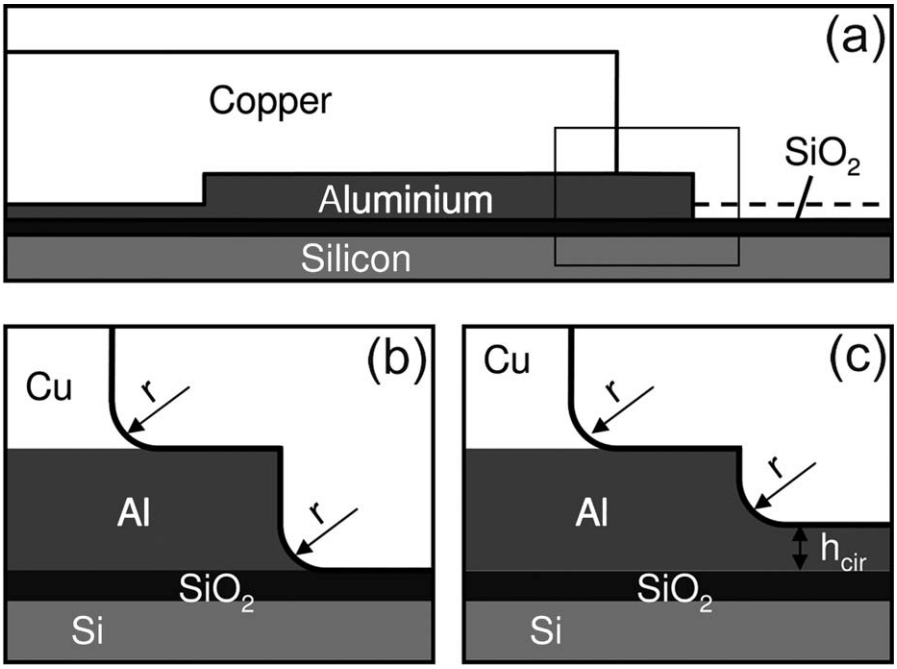

Fig. 3. Description of the two different geometries considered for sub-modelling of the electrode edge. (a) Overall view of the electrode area. (b) and (c) Layer edges in the absence or the presence of Al-interconnects, respectively.

Table 1
Geometry and material parameters employed in the FE model.

Material	Parameter	Symbol	Value
Silicon	Thickness	h_{Si}	115 μm
	Young's modulus	E_{Si}	150 GPa
	Poisson's ratio	ν_{Si}	0.3
Silicon oxide	Thickness	h_{SiO2}	0.66 μm
	Young's modulus	E_{SiO_2}	74 GPa
	Poisson's ratio	ν_{SiO_2}	0.16
Aluminium	Inner thickness	$h_{Al,i}$	1.2 μm
	Outer thickness	$h_{Al,a}$	2.5 μm
	Inner width	$b_{Al,i}$	25 μm
	Outer width	$b_{Al,a}$	5 μm
	Interconnect thickness	h_{cir}	0.7 μm
	Young's modulus	E_{Al}	70 GPa
	Poisson's ratio	ν_{Al}	0.3
Copper	Thickness	h_{Cu}	8 μm
	Diameter	$\varnothing_{Cu}$	110 μm
	Young's modulus	E_{Cu}	130 GPa
	Poisson's ratio	ν_{Cu}	0.3

The pure silicon surface, if put under tension (*i.e.* Si-side), presents a rather wide strength distribution but associated with a higher resistance to failure. The values obtained for Si-side specimens after the Weibull analysis are in good agreement with the results of analyses by previous authors on well-etched surfaces of Si wafers.[3,6,15] On the other hand, for metal-side specimens, the lower strength and much narrower strength distribution (*i.e.* higher m) could be explained by one of (or a combination of) the following mechanisms: (a) presence of a narrow range of large critical defects, most likely caused by etching the silicon surface; (b) presence of a brittle layer due to chemical deposition of the metal contacts; (c) presence of an interfacial structure acting as a stress concentration during biaxial loading; (d) storage of residual stresses in the neighbourhood of the metal contacts. All these mechanisms are associated with the influence of the metal contacts during metal-side testing.

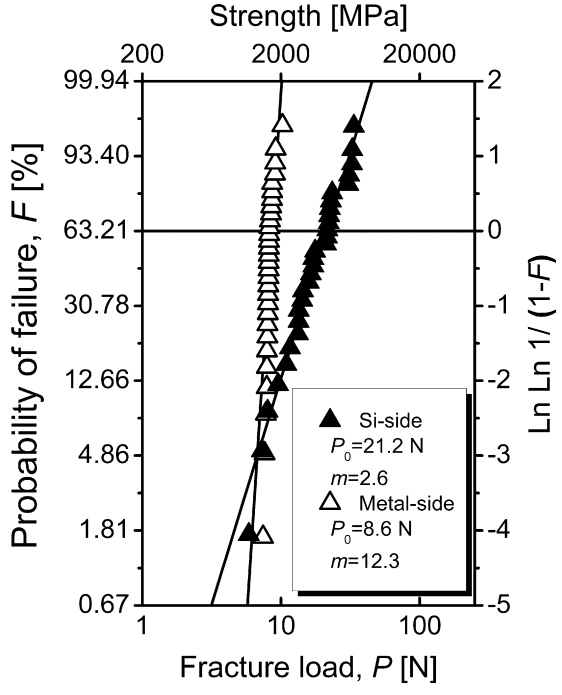

Fig. 4. Fracture load vs. probability of failure plot for Si-chips, obtained with B3B flexure tests. The obtained values of characteristic fracture load for both Si-side ($P_0 = 21.2$ N; $m = 2.6$) and metal-side ($P_0 = 8.6$ N, $m = 12.3$) samples are explicitly reported. The equivalent strength (in MPa) as calculated by Eq. (1) is also indicated.

Table 2
Weibull and fracture mechanical parameters (including 90% confidence intervals) for both Si-side and metal-side Si chips tested with the B3B method.

	Si-side	Metal-side
Characteristic fracture load, P_0 [N]	21.2 [18.6–24.1]	8.6 [8.3–8.8]
Weibull modulus, m	2.6 [2.0–3.2]	12.3 [9.2–15.0]
Equivalent characteristic strength, σ_0 [MPa]	3529 [3099–4025]	1430 [1392–1470]
Critical defect size range, a_c [μm]	0.03–1.0	0.3–0.7
Effective volume, V_{eff} [mm^3]	0.00135	–

3.2. Fracture mechanics analysis of Si-side and metal-side specimens

Based on a linear elastic fracture mechanics (LEFM) approach, the critical defect size (a_c) causing the failure of both Si-side and metal-side loaded specimens can be estimated based on the failure stress, σ_f, and fracture toughness, K_{Ic}, of the material as given by the following equation[4]:

$$a_c = \frac{1}{\pi}\left(\frac{K_{Ic}}{Y\sigma_f}\right)^2, \quad (2)$$

where Y is a dimensionless geometric factor depending on the shape of the defect and loading configuration.

The fracture toughness of silicon single crystals depends on the crystal orientation, the most brittle being the direction ⟨1 1 0⟩ with $K_{Ic} \approx 0.73$ MPa m$^{1/2}$.[16] This fracture toughness value has been taken for the present calculations. Assuming small cracks or embedded circular flaws at or near to the surface, a geometric factor of $Y = 2/\pi$ has been chosen. The range of critical defect sizes calculated with Eq. (2) and based on the failure stress distributions shown in Fig. 4 are reported in Table 2. It can be inferred that the smallest and biggest defects are predicted in the Si-side configuration (*i.e.* between 0.03 μm and 1 μm), whereas in the metal-side case larger critical defects are predicted but within a smaller size range (*i.e.* between 0.3 μm and 0.7 μm). In this regard, we caution the reader that the result of the critical defect size calculation with Eq. (2) might be influenced by the presence of a superimposed stress concentration at the metal–silicon interface. When a stress concentration is present, the effect on the Weibull distribution is the same as that of a high surface roughness. Defects that would not cause fracture on a plain surface for the same applied load become critical in the presence of a localised stress concentration.[3] Consequently, the biaxial strength is lowered and the Weibull modulus increased, compared to the cases where a better surface finish leads to a low

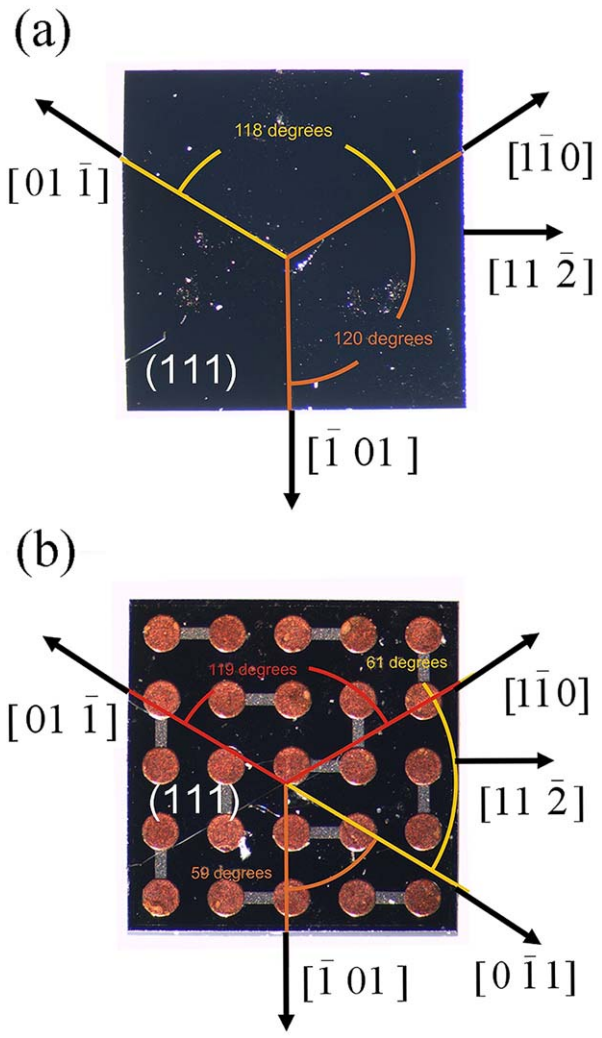

Fig. 5. Preferred fracture directions for (a) Si-side and (b) metal-side specimens tested with the B3B method. Fracture always involves the low-energy {1 1 0} planes intersecting the (1 1 1) plane.

density of large defects.[3,6,15,17] It is thus crucial to distinguish whether the difference in strength and Weibull moduli found between Si-side and metal-side specimens is to be attributed to the presence of larger critical defects or rather to a geometrical effect causing a localised stress concentration. Moreover, residual stresses in the interfacial area of the metal contacts associated with the deposition process could also contribute to lowering the mechanical properties on the metal-side.

3.3. Fractographic investigation of Si-chips

Si-side and metal-side fractured specimens were subjected to EBSD analyses in order to identify the preferred fracture directions. Fig. 5a and b reports planar views of Si chip specimens fractured during Si-side and metal-side testing, respectively. The crystallographic directions along which fracture occurred are explicitly indicated as determined by EBSD. It can clearly be seen that cracks propagated preferentially along ⟨1 1 0⟩ directions, at 60° (or multiples) to one another. This result is in agreement with the {1 1 0} planes being the ones of lowest surface energy (and fracture toughness) among the planes intersecting the (1 1 1) plane.[16,18,19] It should also be remarked from Fig. 5 that, although in the Si-side case the fracture originated at the centre of the sample (where the maximum stress during B3B test occurs), the metal-side specimen (Fig. 5b) presented a fracture origin located at the border of the central metal contact (∼100 μm away from the centre of the specimen), which is probably related to the nature of the metal–silicon interface.

EPMA analyses were performed on cross-sectioned Si chips in order to qualitatively investigate the composition of the metal–silicon interface. The deposited metal contacts consist of a ≈10 μm thick Cu layer. Between the Cu and the silicon an aluminium layer is present, which acts as a buffer layer and interconnect for the Cu contacts.[1] A significant oxygen concentration associated with silicon impoverishment is extensively present across the surface of silicon on the metal-side. This allows us to speculate the possibility that a silicon oxide layer is present, which likely formed over the entire silicon surface that was exposed to an oxidising environment during metal deposition.[20–22] This hypothesis has been corroborated by EPMA analyses performed on the opposite surface of silicon in absence of metal contacts, where no trace of oxygen was found. The rather low spatial resolution (2 μm) of EPMA does not allow us to measure precisely the thickness of the oxide layer. Furthermore, the presence of other submicrometre layers (such as polysilicon[23]) in the interfacial area cannot be excluded. In any case, it could be inferred that since the fracture toughness of silica is lower than that of silicon (≈0.6 MPa $m^{1/2}$ for silica vs. ≈0.8 MPa $m^{1/2}$ for silicon),[14,16] the oxide layer might be responsible for an embrittlement of the Si chips during metal-side biaxial testing.[20] Moreover, the free edges at the end of the Cu and Al layers (perimeter of the metal contact – visible in Fig. 2b) could act as a notch during biaxial loading, which might produce significant stress concentrations.

Fractographic investigations were carried out on several specimens fractured under both Si-side and metal-side configurations. Only specimens which fractured into a small number of pieces (*i.e.* under a low failure load) could be used for microscopic analyses; otherwise they completely fragmented due to the high amount of elastic energy stored during testing. Light microscope images of specimens that failed during biaxial flexural testing with tension on the pure silicon side (Si-side) are depicted in Fig. 6. In both cases, the fracture originated on the silicon side, from what appears to be a relatively large surface defect. The metal contacts (visible in Fig. 6b) are located at the opposite side from where fracture occurred. It is worthy to notice that the hackle lines have a rather asymmetrical shape. This is due to the critical defect being located slightly away from the centre of the specimen, where the maximal stress occurs.[24,25] Fig. 7a and b shows light microscope images of both sides of the fracture plane of a specimen that failed during metal-side B3B testing. As can be inferred from Fig. 7, the fracture originated at the interface between metal and silicon, in the proximity of the border of the metal pad. In Fig. 8 another case of metal-side fracture is presented. The fracture initiation seems to be located in the silicon, exactly below the metal contact, in a peripheral

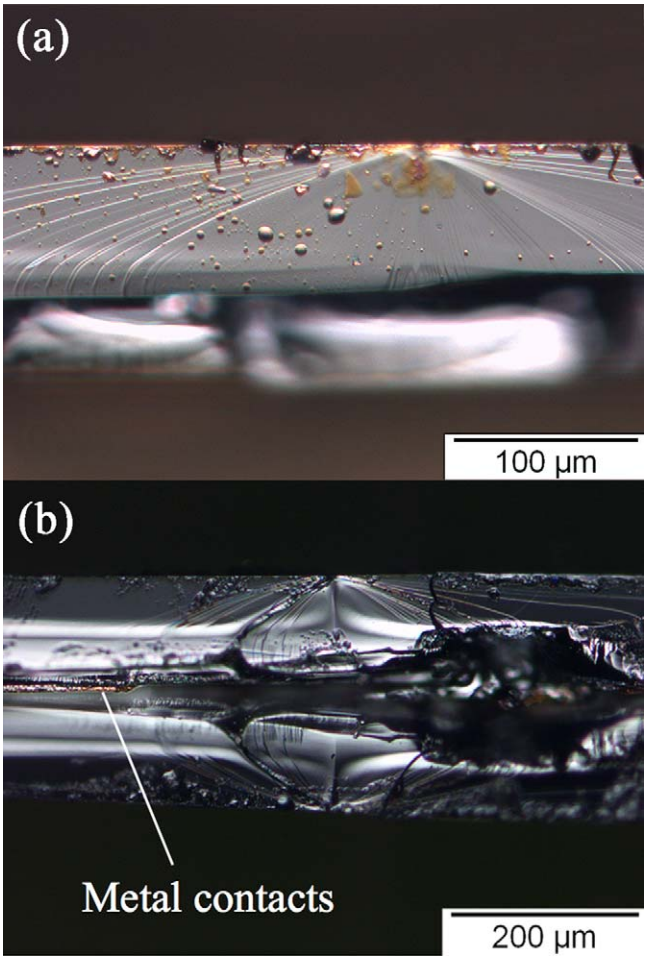

Fig. 6. Microscopic images of the fracture surfaces of Si chips that failed during Si-side B3B testing. Sample in (a) is represented with 20× magnification, whereas sample in (b) with 5× magnification. In (a), the upper side of the sample was subjected to tensile stress. In (b) both fracture surfaces of the same crack are displayed. The fracture originated on the surface free from metal contacts, which was the one put into tension. Since an asymmetrical hackle is present, the critical flaw was likely located away from the centre of load.

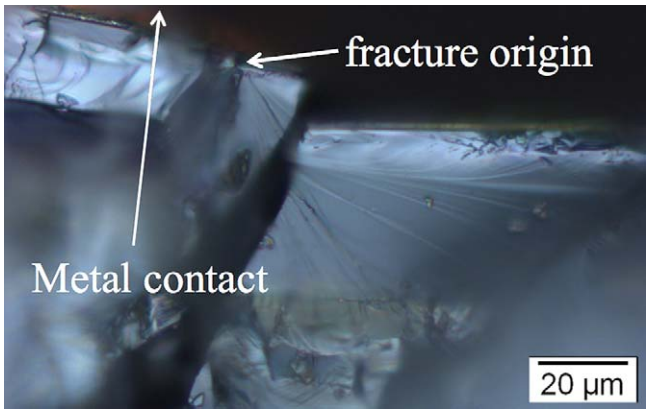

Fig. 8. Microscopic image of the fracture surface of a Si chip that failed during metal-side B3B testing (magnification: 50×). Fracture originated in silicon in proximity of the metal–silicon interface.

position with respect to it. This is in agreement with the other observations.

Fig. 9a displays an SEM picture of a metal-side specimen at a magnification of 5000×. The triangular shape in the middle of the image is located below the upper surface, close to the central metal contact. The presence of the metal contact is witnessed by some remains of the Al buffer layer (as confirmed by simultaneous energy dispersive X-ray analyses). The area where the fracture origin is present is displayed with a higher magnification (20 000×) in Fig. 9b. It is believed that the fracture initiates in the silicon, about 1 μm below the Si–Al interface. The dimension of the critical defect appears to be less than 300 nm, which is the minimum size (see Table 2) predicted for the metal-side specimens by fracture mechanics using Eq. (2). This result suggests the possible involvement of a stress concentration in the fracture process, and allows us to discard the possibility of an etch pit as the critical defect, being the fracture origin located rather in the Si layer.[26]

3.4. FE results of the stress field in the fracture region

The stress distribution in a homogeneous material during biaxial loading (*e.g.* using B3B test) can be numerically evalu-

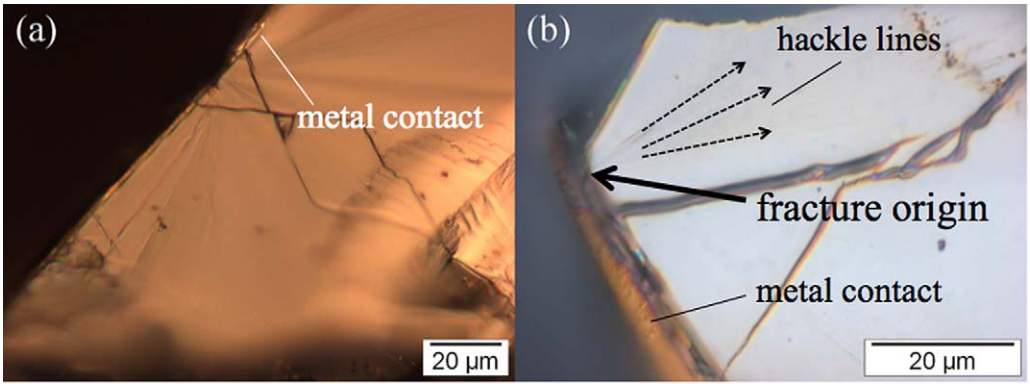

Fig. 7. (a) and (b) Microscopic images of the fracture surface of a Si chip that failed during metal-side B3B testing. Pictures are represented with increasing magnification (50×, 100×) on either side of the fracture plane. Fracture originated in silicon in proximity of the metal–silicon interface. In (b) the direction of hackle lines allows to identify the region where the critical flaw was present.

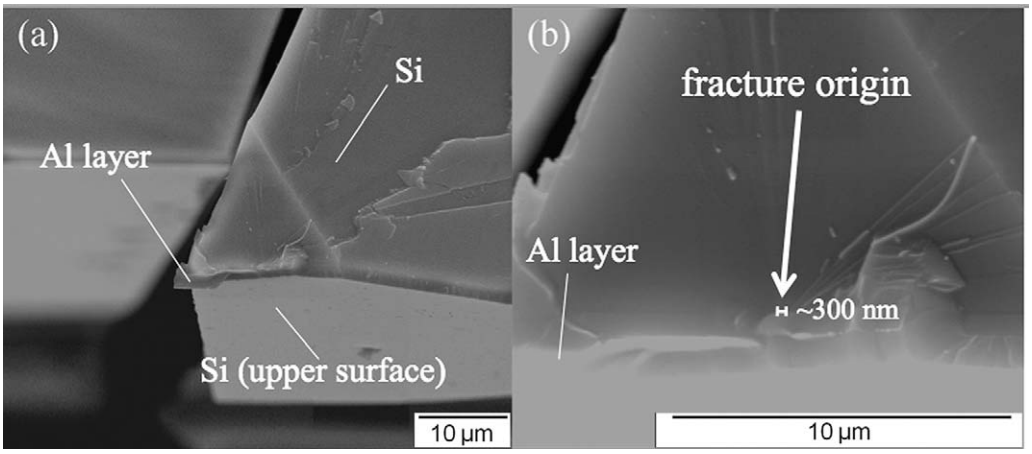

Fig. 9. SEM images of the fracture surface of a Si chip that failed during metal-side B3B testing. Magnification: (a) 5000×, (b) 20 000×. Fracture originated in silicon in proximity of the Al–silicon interface. The size of the critical defect is ≈300 nm.

Table 3
Calculated stress values in the critical points of the metal-silicon interface during metal-side B3B tests. Elements in brackets indicate the phase in which the stress value was calculated.

Location	Position	Stresses without Al-interconnect [MPa]	Stresses with Al-interconnect [MPa]	Reference stress (smooth Si surface) [MPa]
1	Centre of contacts	3249 (Cu)	3243 (Cu)	3000 (Si)
2	Step in Al	1071 (Al)	1083 (Al)	–
3	Cu–Al edge	∞	∞	–
4	Outer edge	∞	∞	–
5	Si below point 4	3260 (Si)	2612 (Si)	–

ated with FE simulations. The maximum stress at failure, σ_{max}, can be calculated using Eq. (1). For the Si-chips studied here, when the metal patterned side is subjected to tension (*i.e.* the metal contacts under tension), several key points may be identified in the geometry of the metal-silicon interface. These can be described as follows (*cf.* Fig. 10a): (1) outer surface of the Cu-contacts, in the middle of the contact pad (*i.e.* in correspondence of the central loading ball), (2) step in the Al layer inside the copper, (3) edge of contacts at the Cu–Al interface, (4) edge of the Al–SiO_2 (Al–Al) interface, and (5) in the silicon, below the edge of the Al–SiO_2 interface. The results of the FE simulations of the biaxial B3B bending test in the interfacial area are also shown in Fig. 10a, while Fig. 10b, c represent close-ups of the edge area in the absence or the presence of the Al-interconnect, respectively. Numerical values corresponding to both configurations are listed in Table 3. The reference stress resulted in ≈3000 MPa, which is the stress value corresponding to a model without metal contacts for an applied reference load of 20 N.[b] The different stress values at the different points will be now compared for the same applied load.

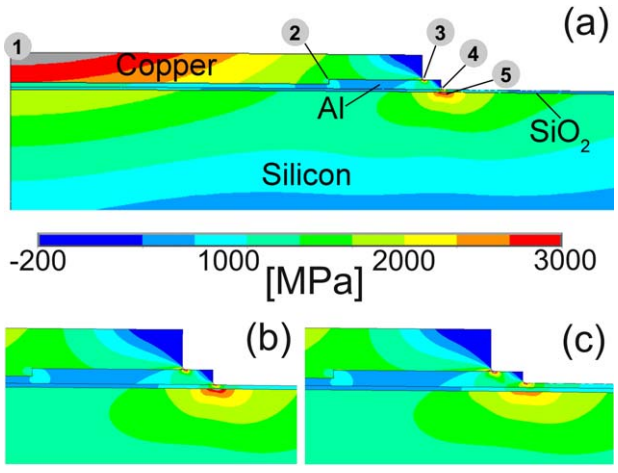

Fig. 10. (a) Location of the critical points in the neighbourhood of Cu contacts and FE results displaying the effect of a metal-side B3B test on the patterned side of Si-chips. (b) and (c) Magnified view of the electrode edges subjected to tensile stress concentration, in the absence or the presence of Al-interconnects, respectively. The same colour scale applies for all the displayed results.

At point 1 (centre of Cu-contact), the maximum biaxial tensile stress results in about 3240 MPa independent of the presence of the Al-interconnect. A similar situation occurs in point 2, where the maximum stress at the step in the Al-layer inside the copper reaches only ca. 1080 MPa. For points 3 and 4, stress concentrations occur both at the Cu–Al edge and at the Al–SiO_2 edge. In the first case, high stresses in Cu or Al will be drastically reduced due to plastic deformation. However, in the SiO_2 and Si regions, being brittle materials, the stresses occurring at points 4 and 5 have to be considered as potentially critical for the chip failure. Due to the stress singularity in point 4, we will concentrate on the corresponding stresses in point 5 in order to compare the

[b] The applied load of 20 N used for the FE simulations corresponds approx. to the fracture load found experimentally.

stress fields in absence and in presence of the Al-interconnect. In Fig. 10b and c it can clearly be seen that the maximum stress in point 5 without the Al-interconnect ($\sigma_{max} = 3260$ MPa) is significantly higher than that resulting when the interconnect is present ($\sigma_{max} = 2612$ MPa).

Based on these results, it becomes evident that the presence of Al-interconnects releases the stress concentration. This is in good agreement with the fractographic experimental observations (*cf.* Figs. 7–9), where failure of the Si-chip always initiates at the border of the central Cu-contact in an area free from Al-interconnects. However, the linear elastic FE simulations cannot predict whether fracture initiates in the silica layer or in the silicon phase. In this regard, although the fracture path was experimentally identified in the Si-phase for all specimens, the possibility that cracks initiate in the SiO_2 layer and then propagate (thus providing an initiation for the fracture in silicon) cannot be ruled out. This could be triggered by the lower toughness of the silica phase and would help to explain the higher Weibull modulus found in the metal-side tested samples. For instance there could be a different defect size distribution within the silica layer, or there could be stable growth of pre-cracks up to the silica-silicon interface (*e.g.* similar to the case of stable crack extension before fracture in multilayer ceramics[27,28]). The investigation of cracks in the very thin silica layer and the detection of other possible layers in the interfacial area exceeds the scope of this work and will be addressed in the near future by means of nanoscale-resolved techniques.

4. Conclusions

The biaxial strength and fracture features of $2\,mm \times 2\,mm \times 0.125\,mm$ Si components for embedding into PCBs have been assessed using a miniaturised ball-on-three-balls testing jig. The results showed a clear statistical difference in the characteristic fracture load when the pure silicon side (Si-side) or metal-patterned side (metal-side) is put into tension, being in the Si-side almost 3 times larger ($P_0 = 21.2$ N) than in the metal-side ($P_0 = 8.6$ N). The Weibull modulus in the Si-side is in agreement with common values for silicon wafers (*i.e.* $m \approx 3$), whereas for the metal-side a very high value is obtained (*i.e.* $m \approx 12$). Fractographic analyses of broken specimens and FE calculations of stress distributions during bending demonstrated that the deposition of additional Al-interconnects around the contacts on the metal-side would lower the stress concentrations and thus optimal designs of miniaturised embedding components could be achieved. The present findings prove that embedding of Si components with different surface features involve significant differences in their fracture load distribution and therefore in their mechanical reliability.

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